IN THE CLAIMS

1. (Canceled)

2. (Currently Amended) The method of Claim ~~1~~ 6 wherein the providing video data comprises:

assigning compression modes to the frames.

3. (Original) The method of Claim 2 wherein the compression modes are selected from a group comprising I-mode, P-mode, and B-mode.

4. (Canceled)

5. (Currently Amended) The method of Claim ~~4~~ 6 wherein the calculating a sigmaSAD value comprises:

calculating a SAD value for each microblock of the second frame;

storing the SAD value in a memory unit for each microblock of the second frame;

calculating the sum of all the SAD values for the second frame; and

dividing the sum by the total number of microblocks of the second frame.

6. (Currently Amended) ~~The method of Claim 4~~ A method for processing digital video signals for live video applications, the method comprising:

providing video data comprising a plurality of frames;

identifying a first frame and a second frame in the frame sequences;

processing information of the first frame and information of the second frame to determine a quantization step value for the second frame; and

adjusting a transmission bit rate for the second frame in response to the quantization step value,

wherein the processing the information of the first frame and the information of the second frame comprises:

calculating a sigmaSAD value for the second frame;

calculating a divisor value for the second frame; and

calculating the quantization step value for the second frame;

and wherein the calculating a divisor value comprises:

selecting a series of integers that is indexed from 0 through n-1;

selecting a complexity integer;

calculating the quotient modulo n of the complexity integer; and

setting the ~~divider~~ divisor value equal to an integer whose index in the series equals the quotient;

wherein n is an integer larger than 1.

7. (Currently Amended) The method of Claim 6 wherein the selecting ~~a~~ the complexity integer comprises:

if the second frame is an I-frame, setting the complexity integer near midrange between an integer A and an integer B; and

if the second frame is not an I-frame, adjusting the complexity integer so that the fullness of a buffer varies toward a predefined fullness level.

8. (Canceled)

9. (Currently Amended) ~~The method of Claim 8~~ A method for processing digital video signals for live video applications, the method comprising:

providing video data comprising a plurality of frames;

identifying a first frame and a second frame in the frame sequences;

processing information of the first frame and information of the second frame to determine a quantization step value for the second frame; and

adjusting a transmission bit rate for the second frame in response to the quantization step value,

wherein the processing the information of the first frame and the information of the second frame comprises:

calculating a sigmaSAD value for the second frame;

calculating a divisor value for the second frame; and

calculating the quantization step value for the second frame;

wherein the calculating the quantization step value comprises setting the quantization step value equal to the sum of the ratio of the sigmaSAD value to the divisor value and a ~~wherein the~~ constant ~~equals~~ equal to 1.

10. (Currently Amended) The method of Claim ~~1~~ 6 wherein the processing the information of the first frame and the information of the second frame comprises:

deciding whether to encode a frame in the I-mode before any P-frame encoding is accomplished.

11. (Original) The method of Claim 6 wherein the processing comprises:

adjusting the complexity integer so that the size of encoded data for any one of the plurality of frames has approximately an equal size.

12. (Currently Amended) The method of Claim ~~1~~ 6 wherein the method for processing digital video signals further comprises:

determining the locations of I-frames in the step of providing video data;

extending frames immediately preceding the I-frames for one additional frame time; and

skipping frames immediately following the I-frames.

13-14. (Canceled)

15. (Currently Amended) The ~~code~~ system of claim ~~14~~ 16 wherein the code that calculates ~~a~~ the sigmaSAD value comprises:

code that calculates a SAD value for each microblock of the second frame;

code that stores the SAD value in a memory unit for each microblock of the second frame;

code that calculates the sum of all the SAD values for the second frame; and

code that divides the sum by the total number of microblocks of the second frame.

16. (Currently Amended) ~~The code system of claim 14~~ A system including a processor for processing digital video signals for live video applications, the system comprising:

a memory unit within which a computer program is stored, the computer program comprising:

code that instructs the processor to receive video data comprising a plurality of frames;

code that directs the processor to identify a first frame and a second frame in the frame sequences; and

code that directs the processor to process the information of the first frame and the information of the second frame to determine a quantization step value for the second frame, wherein the code that directs the processor to process the information of the first frame and the information of the second frame comprises:

code that calculates a sigmaSAD value for the second frame;

code that calculates a divisor value for the second frame; and

code that calculates the quantization step value for the second frame,

wherein the code that calculates ~~a~~ the divisor value comprises:

code that selects a series of integers that is indexed from 0 through n-1;

code that selects a complexity integer;

code that calculates the quotient modulo n of the complexity integer; and

code that sets the ~~divider~~ divisor value equal to an integer whose index in the series equals the quotient;

wherein n is an integer larger than 1.

17. (Currently Amended) The ~~code~~ system of claim 16 wherein the code that selects ~~a~~ the complexity integer comprises:

code that sets the complexity integer near midrange between an integer A and an integer B if the second frame is an I-frame; and

code that adjusts the complexity integer so that the fullness of a buffer varies toward a predefined fullness level if the second frame is not an I-frame.

18. (Canceled)

19. (Currently Amended) The system of claim ~~18~~ 20 wherein the sigmaSAD calculation ~~subsystem~~ subsystem comprises:

a subsystem that calculates a SAD value each microblock of a frame of the plurality of frames;

a subsystem that stores the SAD value in a memory unit for each microblock of the frame;

a subsystem that calculates the sum of all the SAD values for the frame; and

a subsystem that divides the sum by the total number of microblocks of the frame.

20. (Currently Amended) ~~The system of claim 18~~ A system for processing digital video signals for live video applications, the system comprising:

a video providing subsystem that provides video data comprising a plurality of frames;

a sigmaSAD calculation subsystem that calculates a value of sigmaSAD; and

a divisor calculation subsystem that calculates a value of the divisor, wherein the divisor calculation subsystem comprises:

a subsystem that selects a series of integers that is indexed from 0 through n-1;

a subsystem that selects a complexity integer;

a subsystem that calculates the quotient modulo n of the complexity integer; and

a subsystem that sets the ~~divider~~ divisor value equal to an integer whose index in the series equals the quotient;

wherein n is an integer larger than 1.

21. (Currently Amended) The system of claim 20 wherein the subsystem that selects ~~a~~ the complexity integer comprises:

a subsystem that if the second frame is an I-frame, sets the complexity integer near midrange between an integer A and an integer B; and

a subsystem that if the second frame is not an I-frame, adjusts the complexity integer so that the fullness of a buffer varies toward a predefined fullness level.

22. (Currently Amended) The system of claim ~~18~~ 20 further ~~comprises~~ comprising:

a quantization step calculation subsystem that sets the quantization step equal to the sum of the ratio of the value of sigmaSAD to the value of the divisor, and a constant.

Objection to the Drawings

The drawings are objected to because "figures 1, 3, 4, 6, and 7 are the same and the Examiner does not see the need to have all the drawings." Applicant disagrees.

First, although at first glance figures 1, 3, 4, 6, and 7 appear to be the same, corresponding similar elements of figures 1, 3, 4, 6, and 7 represent different embodiments of the present invention, and therefore are labeled with different reference numbers to indicate that corresponding steps/elements of the various embodiments may be implemented differently.

Second, Applicant is not aware of any requirement in the patent regulations (e.g., 37 CFR) that forbids the number of figures that may be provided in a patent application, nor has the Examiner pointed to any such requirement.

Accordingly, Applicant respectfully submits that the figures are in compliance with the relevant provisions of 37 CFR, and requests the Examiner to withdraw the objection to the drawings.

Objection to Claims

Claims 6-7, 9, 11, 16-17, and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Claim 6 is amended to include all of the limitations of base Claim 1 and intervening Claim 4, and is therefore now allowable. Claims 7 and 11 depend from Claim 6 and therefore distinguish over the cited art for at least the same reasons as Claim 6.

Claim 9 is amended to include all of the limitations of base Claim 1 and intervening Claims 4 and 8, and is therefore now allowable.

Claim 16 is amended to include all of the limitations of base Claim 13 and intervening Claim 14, and is therefore now allowable. Claim 17 depends from Claim 16 and therefore distinguishes over the cited art for at least the same reasons as Claim 16.

Claim 20 is amended to include all of the limitations of base Claim 18, and is therefore now allowable. Claim 21 depends from Claim 20 and therefore distinguishes over the cited art for at least the same reasons as Claim 20.

Rejection of Claims under 35 USC §102

Claims 1-5, 8, 10, 13-15, 18-19, and 22 are rejected under 35 USC §102(e) as anticipated by U.S. Patent No. 6,539,124 to Sethuraman et al.

Claims 1, 4, 8, 13, 14, and 18 are canceled, and therefore their rejections are now moot.

Claims 2-3, 5, and 10-11 depend from Claim 6, which as indicated above is allowable, and therefore Claims 2-3, 5, and 10-11 distinguish over the cited references for at least the same reasons as Claim 6.

Claim 15 depends from Claim 16, which as indicated above is allowable, and therefore Claim 15 distinguishes over the cited references for at least the same reasons as Claim 16.

Claims 19 and 22 depend from Claim 20, which as indicated above is allowable, and therefore Claims 19 and 22 distinguish over the cited references for at least the same reasons as Claim 20.

Rejection of Claims under 35 USC §103

Claim 12 is rejected under 35 USC §103 as being obvious in view of U.S. Patent No. 6,539,124 to Sethuraman et al.

As indicated above, Claim 12 depends from Claim 6, which is allowable, and therefore Claim 12 distinguishes over the cited references for at least the same reasons as Claim 6.